



FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
0077.20 (1778.0120002)APPLICATION NO.
09/364,786APPLICANT
Thekkath *et al.*FILING DATE
July 30, 1999GROUP
2672

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
DZL	AA1	5,619,198	04/1997	Blackham <i>et al.</i>			
DZL	AB1	6,175,907	01/2001	Elliott <i>et al.</i>			
	AC1						
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	AH1						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DZL	AR	1	MIPS IV Instruction Set (R10000), Revision 3.2, MIPS Technologies, Inc., entire publication submitted (September, 1995).
DZL	AS	1	MIPS RISC Architecture - Volume I - Introduction to the ISA, MIPS Technologies, Inc., entire publication submitted (August, 1998).
DZL	AT	1	MIPS RISC Architecture - Volume II - The Instruction Set, MIPS Technologies, Inc., entire publication submitted (August, 1998).

EXAMINER

Daniel Chang

DATE CONSIDERED

2/7/03

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	AA2						
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	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DZL	AR	2	Kubosawa, H. <i>et al.</i> , "Four-way VLIW Geometry Processor for 3D Graphics Applications," <i>FUJITSU Sci. Tech. J.</i> , 36, 1, pp.39-47 (June 2000) (manuscript received December 1, 1999).
DZL	AS	2	Thekkath <i>et al.</i> , "An Architecture Extension for Efficient Geometry Processing," slides 1-23, presented at Hot Chips 11, A Symposium of High-Performance Chips, Stanford Univ. (August 1999) (submitted for conference review July 14, 1999).
DZL	AT	2	Uhler, M., "Optimizing Game Applications for the MIPS RISC Architecture," <i>Computer Game Developer's Conference</i> , San Jose, CA, 14 pages (March 1999) (submitted for conference review on 2/12/99).

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	AA3						
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	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

D7C	AR	3	Uhler, M., "Optimizing Game Applications for the MIPS RISC Architecture," Computer Game Developer's Conference, San Jose, CA, slides 1-22 (March 1999).
D7C	AS	3	Altivec™ Technology Fact Sheet, Motorola, Inc., 2 pages (1998).
D7C	AT	3	Altivec™ Technology Programming Environment's Manual, Rev. 0.1, Motorola, Inc., entire document submitted (November 1998).

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	AA4						
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	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DZC	AR	4	Altivec™ Technology Programming Interface Manual, Rev. 0, Motorola, Inc., entire document submitted (June 1999).
DZC	AS	4	Fuller, S., "Motorola's Altivec™ Technology" [white paper], Motorola, Inc., 4 pages (1998).
bzc	AT	4	Diefendorff et al., "Altivec Extension to PowerPC Accelerates Media Processing," IEEE Micro, pp. 85-95 (March/April 2000).

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	AA5						
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	AL5						Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

D71	AR	5	AltVec™ Technology Programming Environments Manual, Preliminary Rev. 0.2, Motorola, Inc., pp. i-viii, xi-xviii, 1-1 thru 1-11, 4-16 thru 4-33, 6-82, 6-122, 6-135, and 6-143 (May 1998).
D72	AS	5	3DNow™ Technology Manual, Advanced Micro Devices, Inc., entire document submitted (72 pages total) (May 1998).
D73	AT	5	Copy of Office Action from U.S. Patent Application No. 09/249,177, filed February 12, 1999, 10 pages, mailed June 21, 2000.

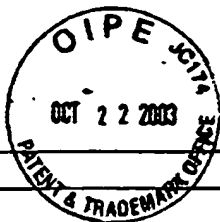
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	AA6						
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	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (including Author, Title, Date, Pertinent Pages, etc.)

D7C	AR	6	Rice <i>et al.</i> , "Multiprecision division on an 8-bit processor," Computer Arithmetic, 1997, Proceedings, 13 th IEEE Symposium on 6-9 July 1997, pp. 74-81.
	AS	6	
	AT	6	

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